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## AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (previously presented) An integrated circuit (IC) comprising:

a plurality of devices connected together and forming circuits;

a switchable current source selectively providing a known current to a PN junction in at least one of said plurality of devices, said switchable current source comprising:

a constant current source, and

a clamping device selectively shunting current from said constant current source; and

a voltage measurement circuit measuring voltage across said PN junction, measured said voltage corresponding to PN junction temperature.

2. (canceled)

3. (original) An IC as in claim 1, wherein said voltage measurement circuit comprises an analog to digital converter.

4. (original) An IC as in claim 1, wherein said voltage measurement circuit comprises a comparator.

5. (original) An IC as in claim 4, wherein a reference voltage is provided to said comparator for comparison against said voltage across said PN junction.

6. (original) An IC as in claim 1, wherein said plurality of devices includes a plurality of field effect transistors (FETs) and said PN junction is a FET body to source/drain junction.

7. (original) An IC as in claim 6, wherein said IC is on a silicon on insulator chip and said plurality of FETs comprises a plurality of P-type FETs (PFETs) and a plurality of N-type FETs (NFETs) connected together in CMOS circuits.

8. (canceled).

9. (previously presented) An IC as in claim 7, wherein said voltage measurement circuit comprises an analog to digital converter.

10. (previously presented) An IC as in claim 7, wherein said voltage measurement circuit comprises a comparator.

11. (original) An IC as in claim 10, wherein a reference voltage is provided to said comparator for comparison against said voltage across said PN junction.

12 – 31 (canceled)

32. (previously presented) An IC as in claim 6, wherein said FET body is P-type silicon body layer in a NFET and said NFET is in a CMOS inverter.

33. (previously presented) An IC as in claim 32, wherein said CMOS inverter is an inverter in a ring oscillator.

34. (previously presented) An IC as in claim 33, wherein said ring oscillator comprises a NAND gate connected in series with a plurality of inverters, said inverter being one of

said plurality of inverters, an output of said NAND gate being in phase with an output of said inverter.

35. (previously presented) An IC as in claim 34, wherein said clamping FET is a NFET and an input of said NAND gate is connected to the gate of said clamping NFET, whereby a gating signal to said input selectively turns said clamping NFET off and blocks oscillation of said ring oscillator.

36. (previously presented) An IC as in claim 35, wherein said voltage is provided to a comparator, said comparator comparing said voltage against a reference voltage.

37. (currently amended) An IC as in claim 1, wherein said clamping device is [[in]] parallel with said constant current source.

38. (previously presented) A CMOS integrated circuit (IC) comprising:

a plurality of field effect transistors (FETs) forming CMOS circuits;

at least one CMOS circuit comprising:

a constant current source, and

a clamping device selectively shunting current from said constant current source to a PN junction in one FET in said at least one CMOS circuit; and

a voltage measurement circuit measuring voltage across said PN junction, measured said voltage corresponding to PN junction temperature.

39. (previously presented) A CMOS IC as in claim 38, wherein said voltage measurement circuit comprises an analog to digital converter.

40. (previously presented) A CMOS IC as in claim 38, wherein said voltage measurement circuit comprises a comparator and a reference voltage is provided to said comparator for comparison against said voltage across said PN junction.

41. (previously presented) A CMOS IC as in claim 38, wherein said PN junction is a FET body to source/drain junction.

42. (previously presented) A CMOS IC as in claim 41, wherein said CMOS IC is on a silicon on insulator (SOI) IC chip.

43. (previously presented) A CMOS IC as in claim 42, wherein said FET body is P-type silicon body layer in a NFET and said NFET is in a CMOS inverter.

44. (previously presented) A CMOS IC as in claim 43, wherein said CMOS inverter is an inverter in a ring oscillator.

45. (previously presented) A CMOS IC as in claim 44, wherein said ring oscillator comprises a NAND gate connected in series with a plurality of inverters, said inverter being one of said plurality of inverters, an output of said NAND gate being in phase with an output of said inverter.

46. (previously presented) A CMOS IC as in claim 45, wherein said clamping FET is a NFET in parallel with said constant current source and an input of said NAND gate is connected to the gate of said clamping NFET, whereby a gating signal to said input selectively turns said clamping NFET off and blocks oscillation of said ring oscillator.

47. (currently amended) A CMOS silicon on insulator (SOI) integrated circuit (IC) chip comprising:

a plurality of field effect transistors (FETs) connected to form a plurality of CMOS circuits, said plurality of CMOS circuits including a plurality of inverters; and

a ring oscillator including series connected ones of said plurality of inverters, at least one inverter of said ones comprising:

a constant current source, and

a clamping device in parallel with said constant current source selectively shunting current from said constant current source to a FET body to source/drain junction in said at least one CMOS circuit; and

a voltage measurement circuit measuring voltage across said PN junction, measured said voltage corresponding to PN junction temperature, wherein said FET body is P-type silicon body layer in a NFET and wherein said ring oscillator further comprises a NAND gate connected in series with said ones, an output of said NAND gate being in phase with an output of said at least one inverter.

48. (canceled)

49. (currently amended) A CMOS SOI IC chip as in claim 47 [[48]], wherein said clamping FET is a NFET and an input of said NAND gate is connected to the gate of said clamping NFET, whereby a gating signal to said input selectively turns said clamping NFET off and blocks oscillation of said ring oscillator.

50. (previously presented) A CMOS SOI IC chip as in claim 47, wherein said voltage measurement circuit comprises an analog to digital converter.

51. (previously presented) A CMOS SOI IC chip as in claim 47, wherein said voltage measurement circuit comprises a comparator and a reference voltage is provided to said comparator for comparison against said voltage across said PN junction.